

**FIG. 1**

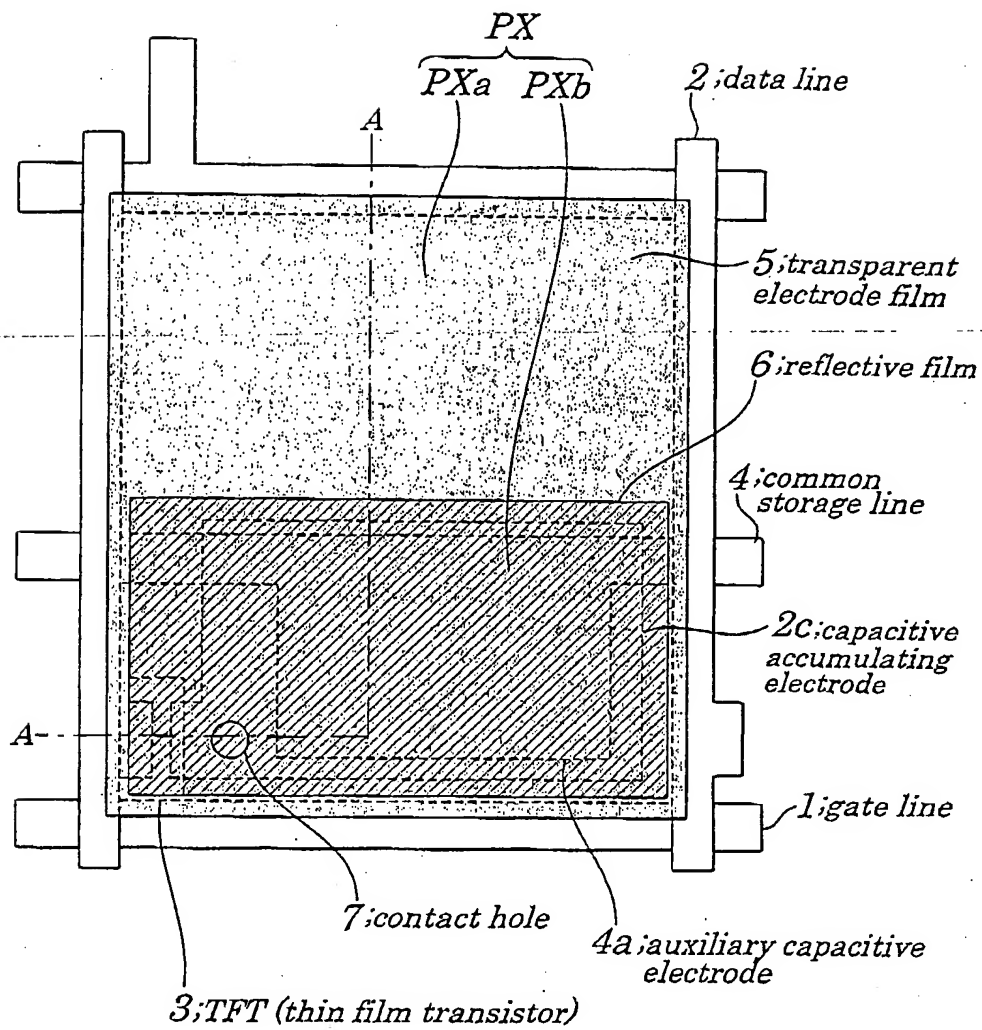
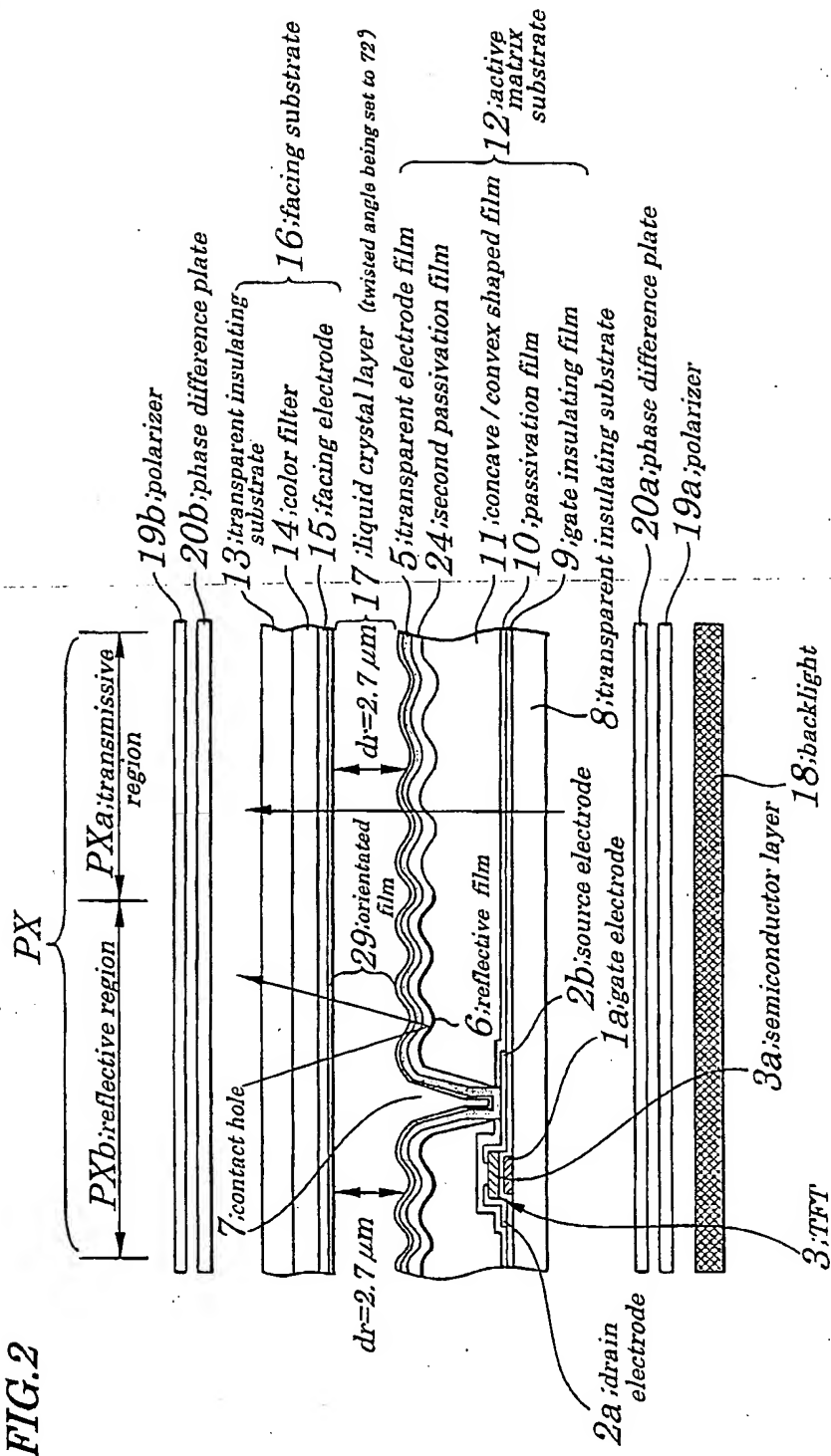
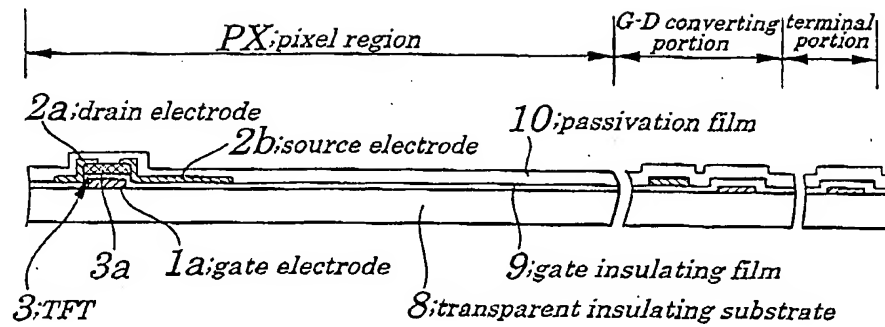


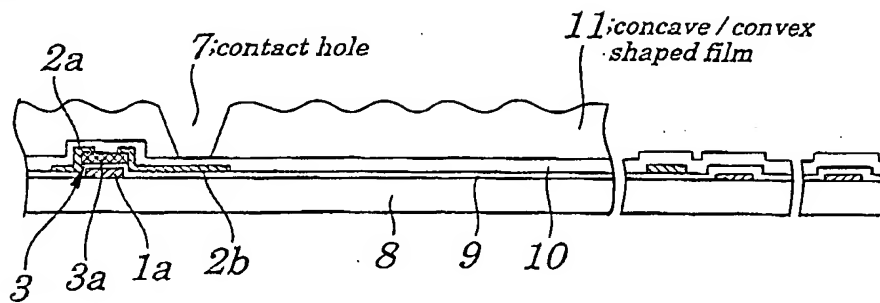
FIG. 2



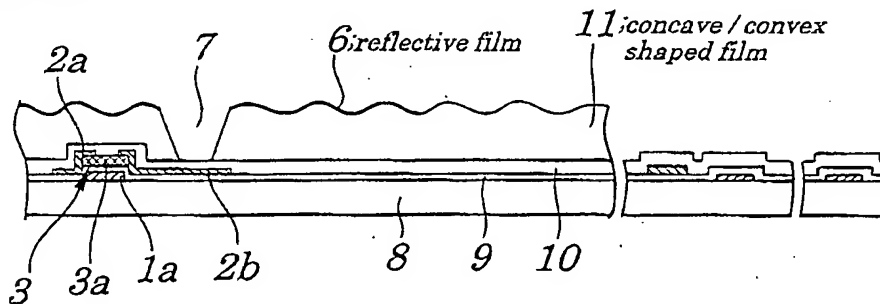
**FIG. 3A**



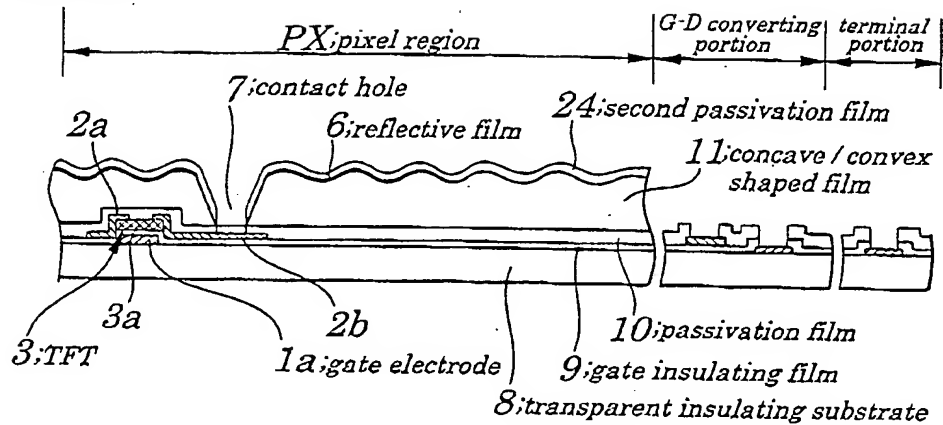
**FIG. 3B**



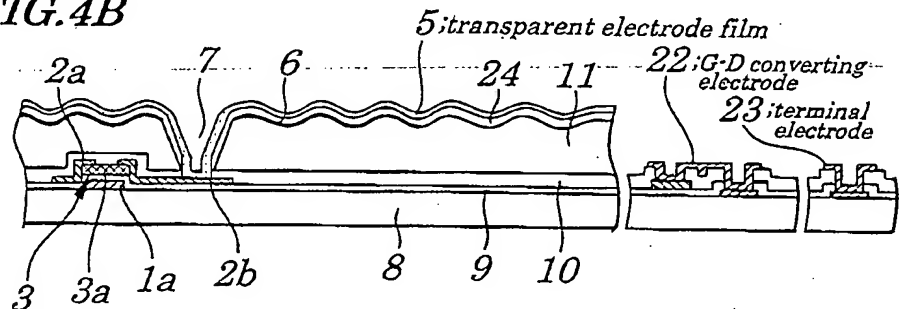
**FIG. 3C**



**FIG. 4A**



**FIG. 4B**



**FIG. 5**

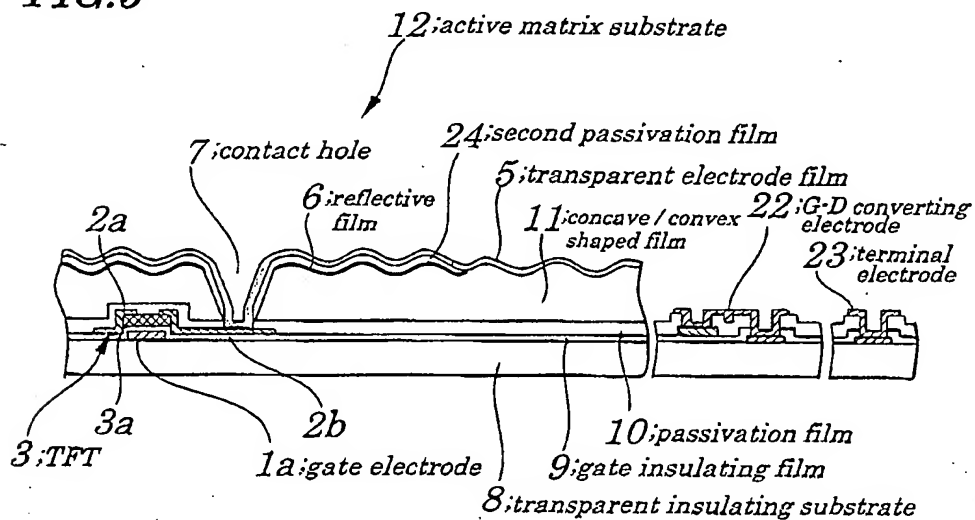


FIG. 6

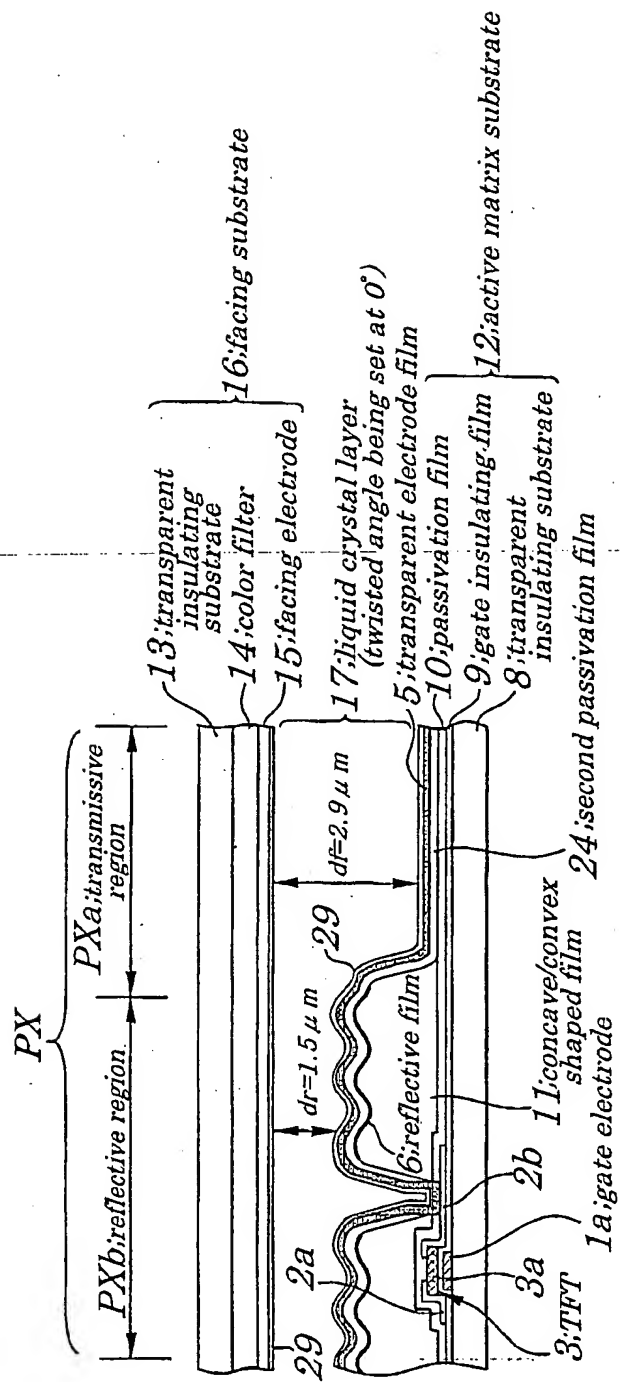
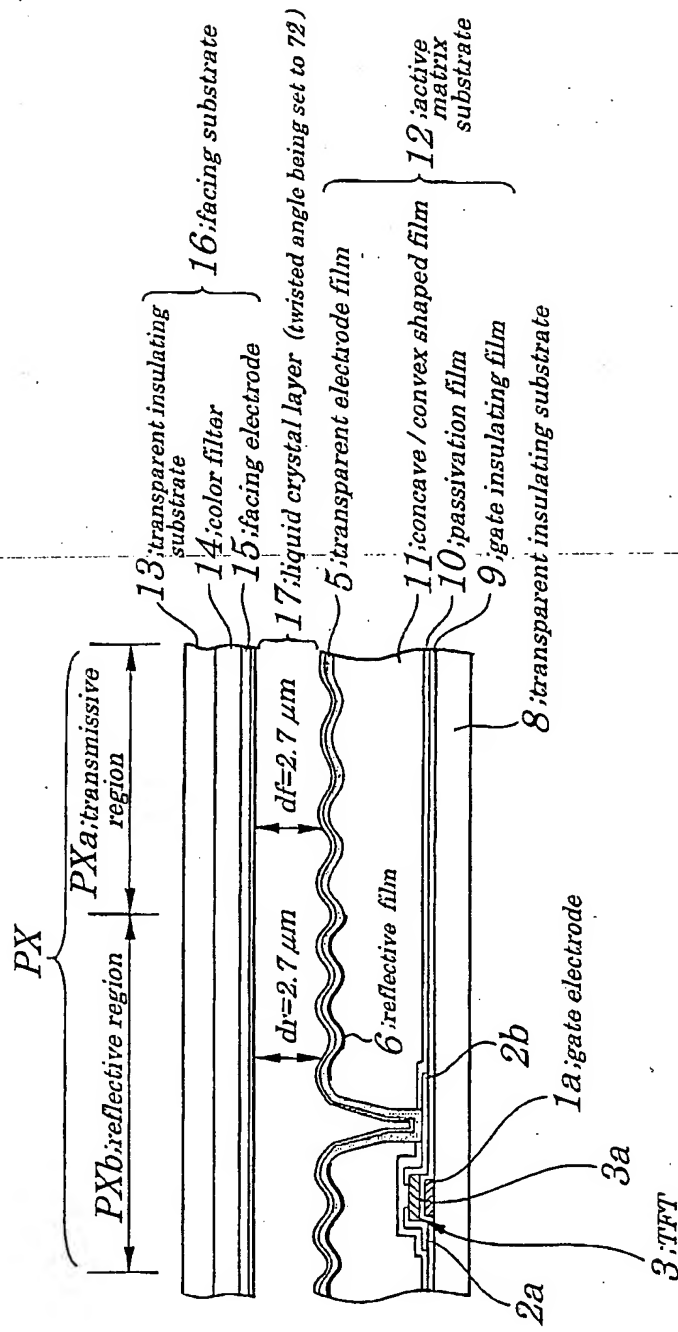




FIG. 8

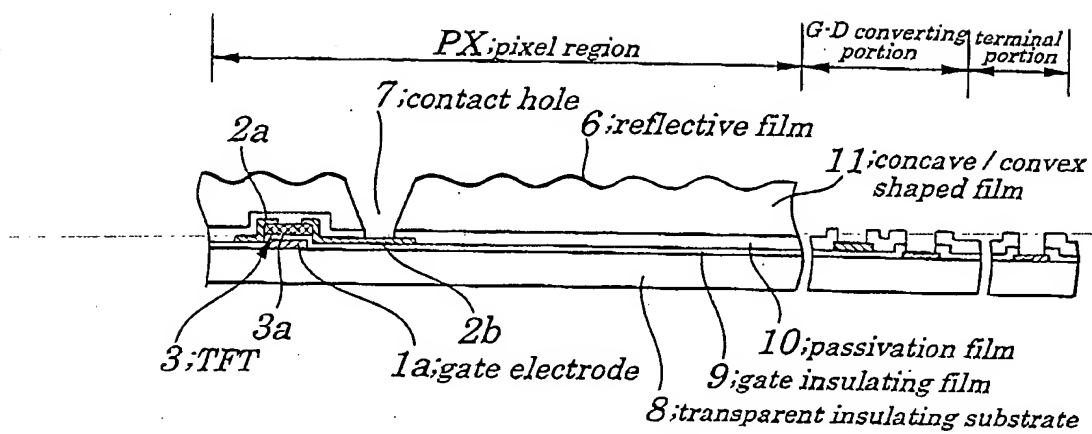


This diagram shows a cross-sectional view of the first embodiment of the TFT array substrate. The structure is divided into three main regions: a pixel region (PX) on the left, a gate-drain (G-D) converting portion in the middle, and a terminal portion on the right. The pixel region contains a TFT structure with a drain electrode (2a), a source electrode (2b), and a gate electrode (1a). The G-D converting portion and terminal portion also show similar electrode structures. The entire structure is built on a transparent insulating substrate (8) and covered by a passivation film (10). A gate insulating film (9) is located beneath the electrodes. A TFT element (3) is also indicated in the pixel region.

Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate with a concave/convex shaped film (11) on top. A contact hole (7) is formed in the film. A conductive layer (2a) is deposited in the hole, and another layer (2b) is on top of it. A layer (3) is on the substrate, with a sub-layer (3a) under the contact hole. Other layers are labeled 1a, 8, 9, and 10. The device is shown in a row of three.



**FIG.10A**



**FIG.10B**

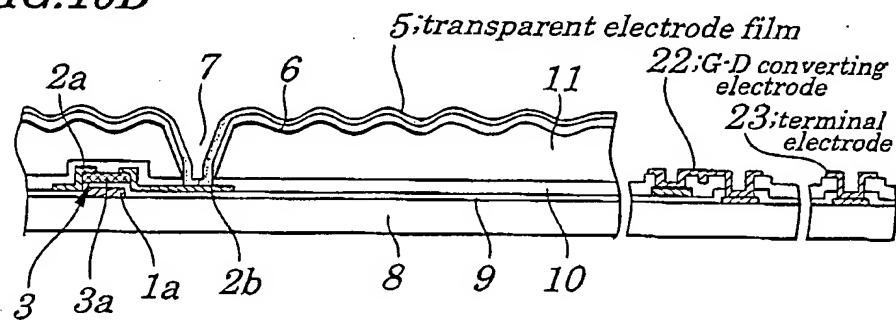


FIG. 11

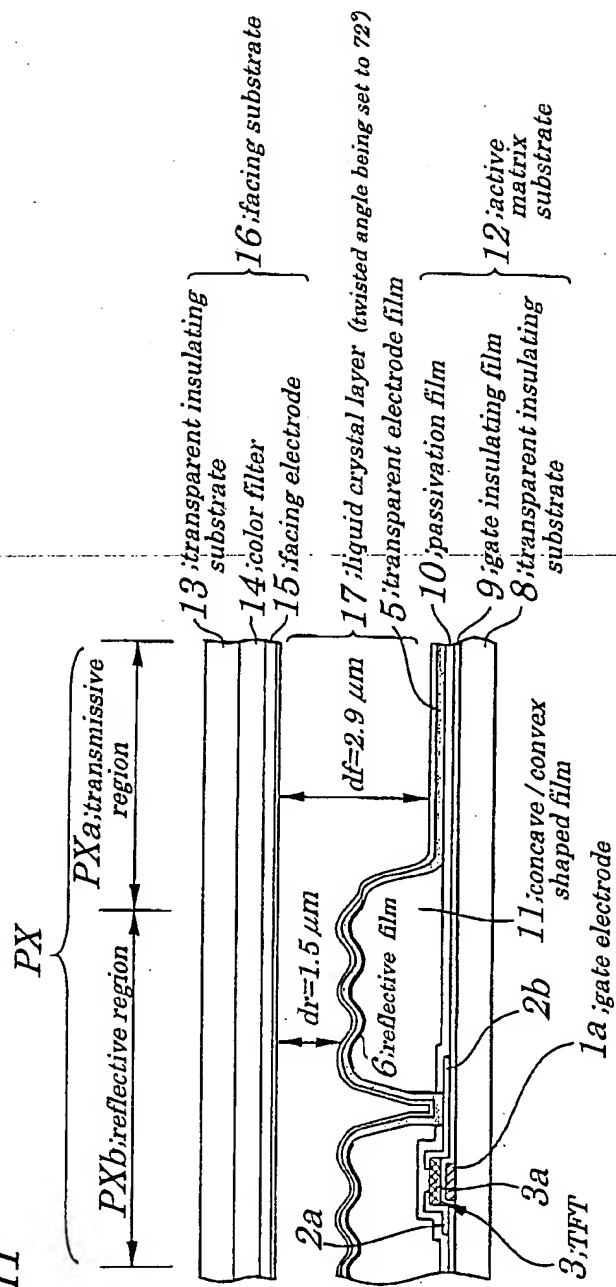


FIG. 12

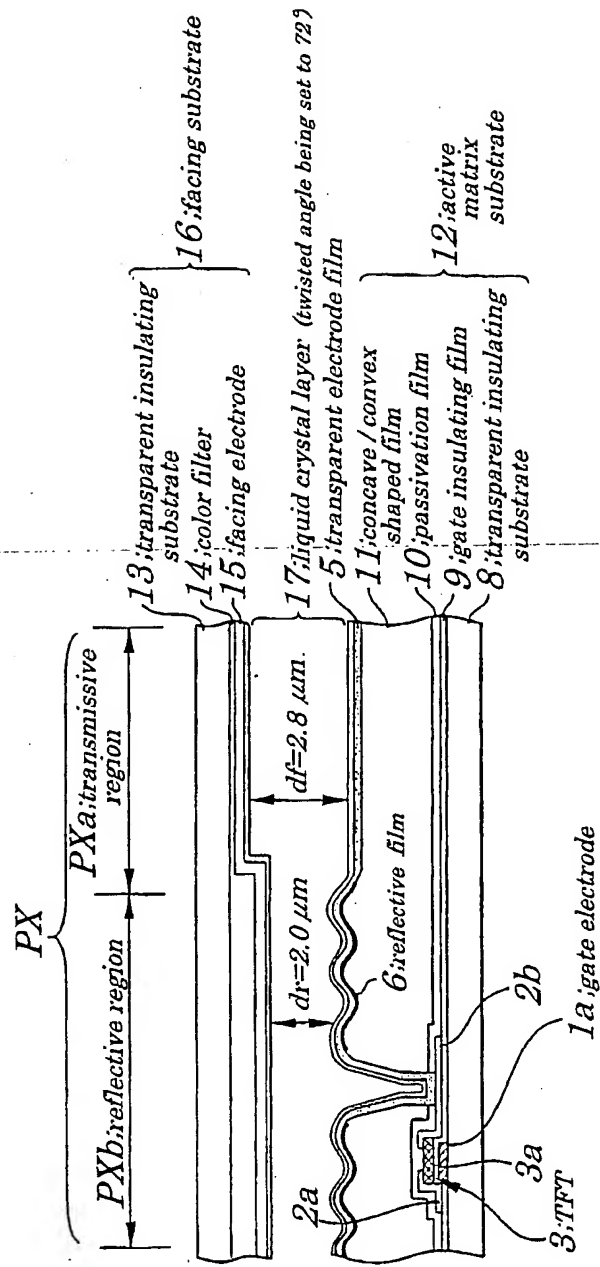
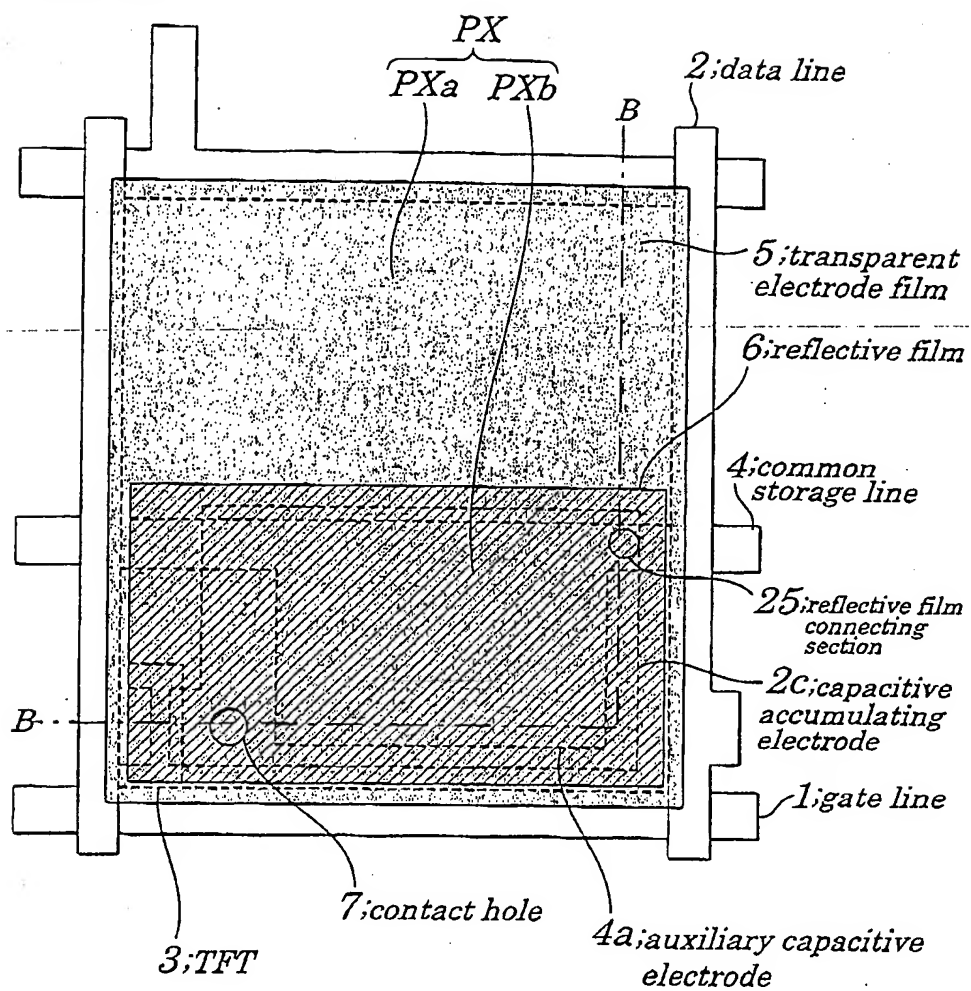
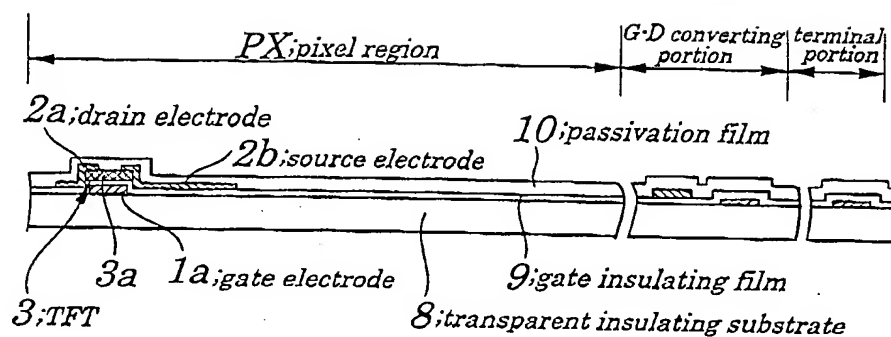


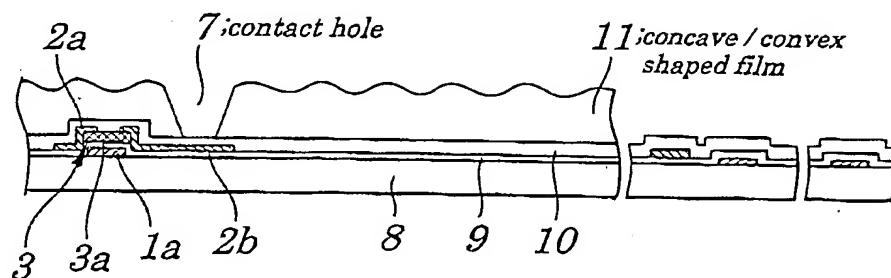
FIG.13



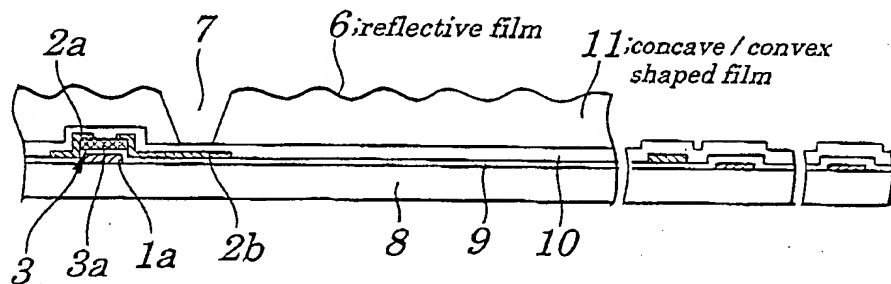
**FIG.14A**



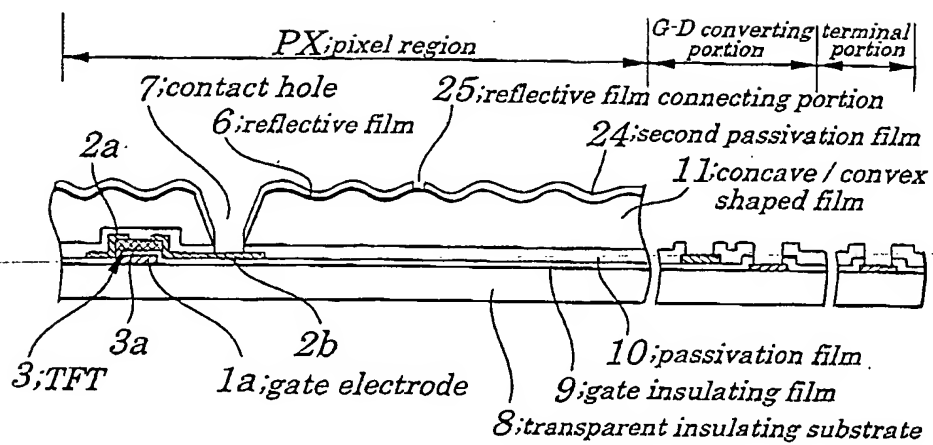
**FIG.14B**



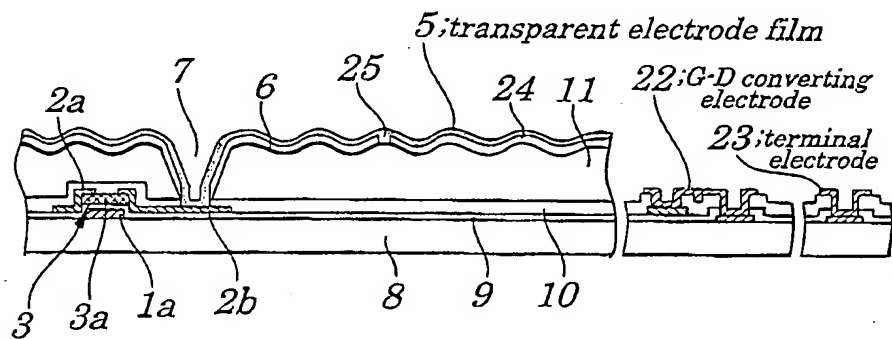
**FIG.14C**



*FIG. 15A*



**FIG. 15B**



*FIG. 16*

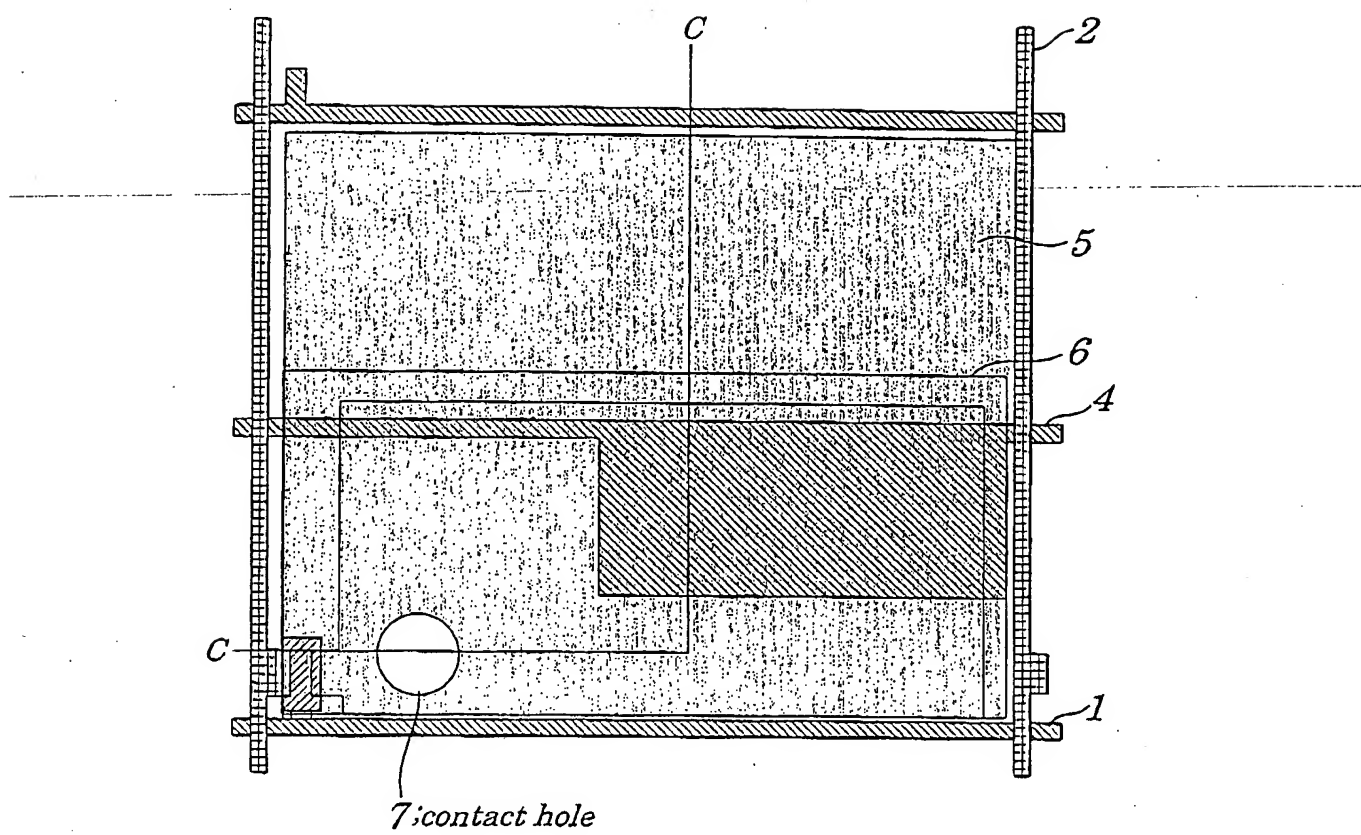
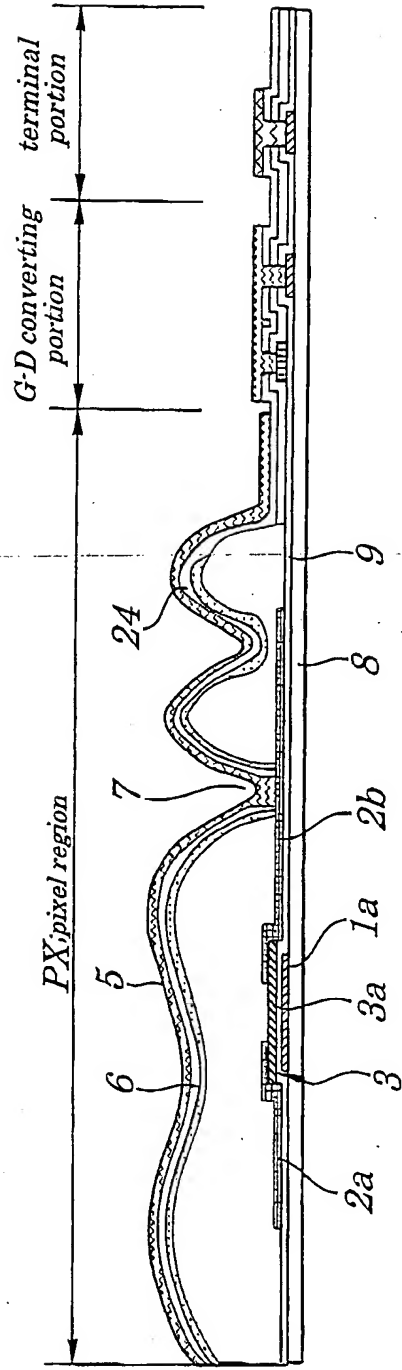
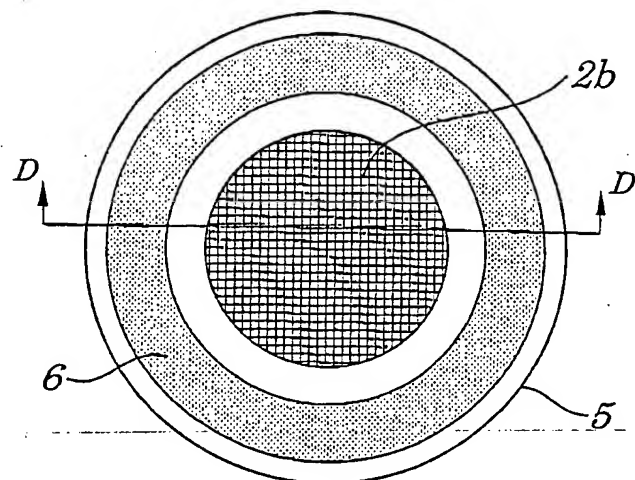


FIG. 17

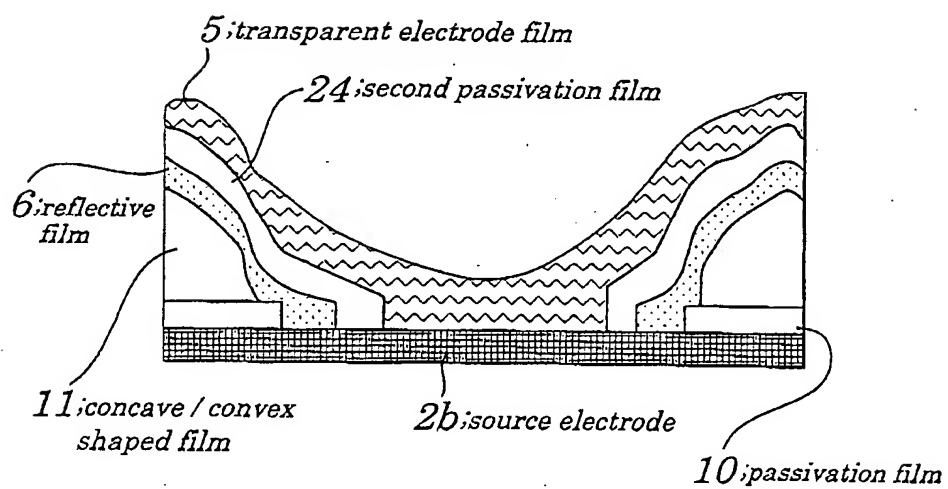




**FIG.18**



**FIG.19**



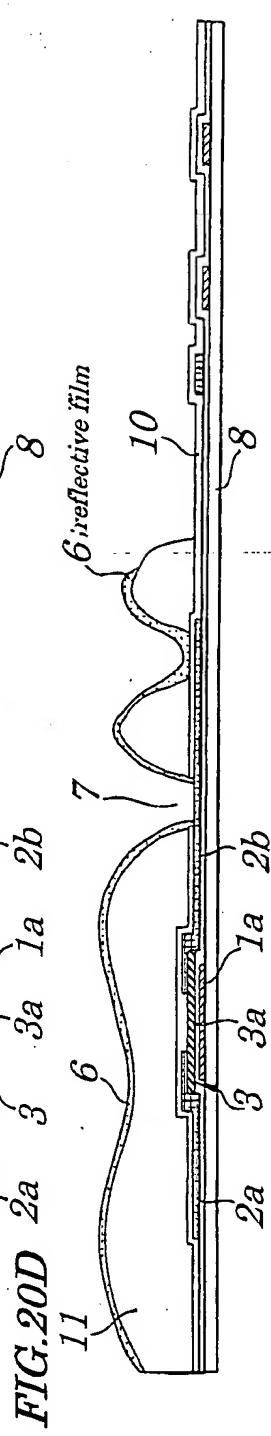
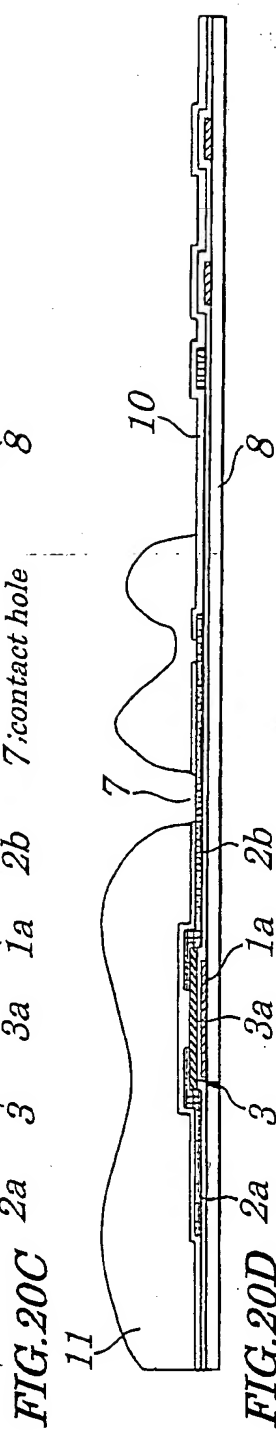
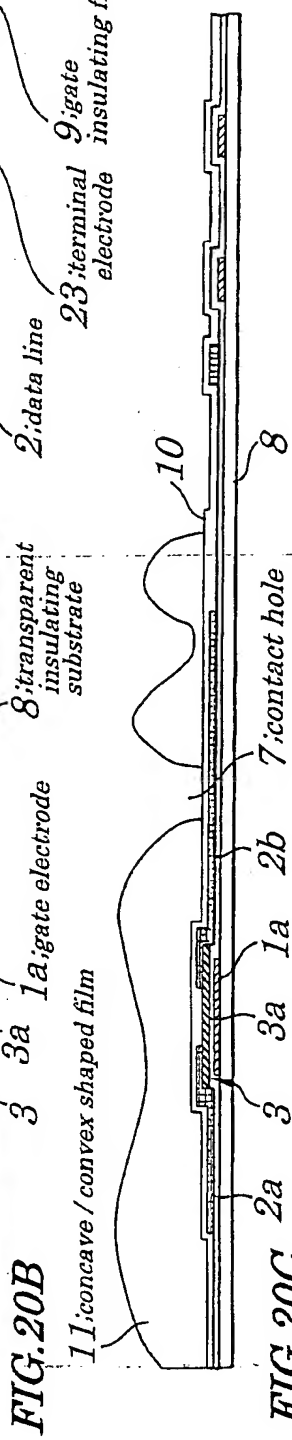
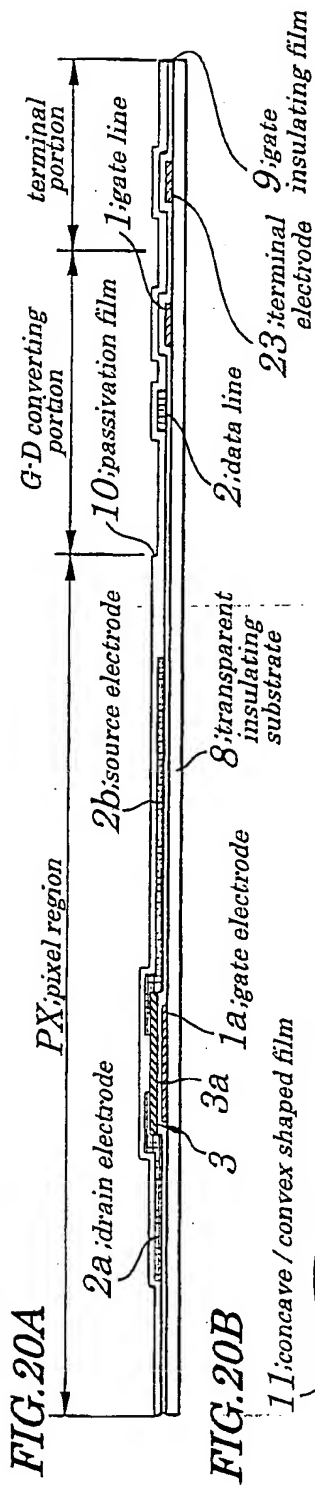


FIG. 21A

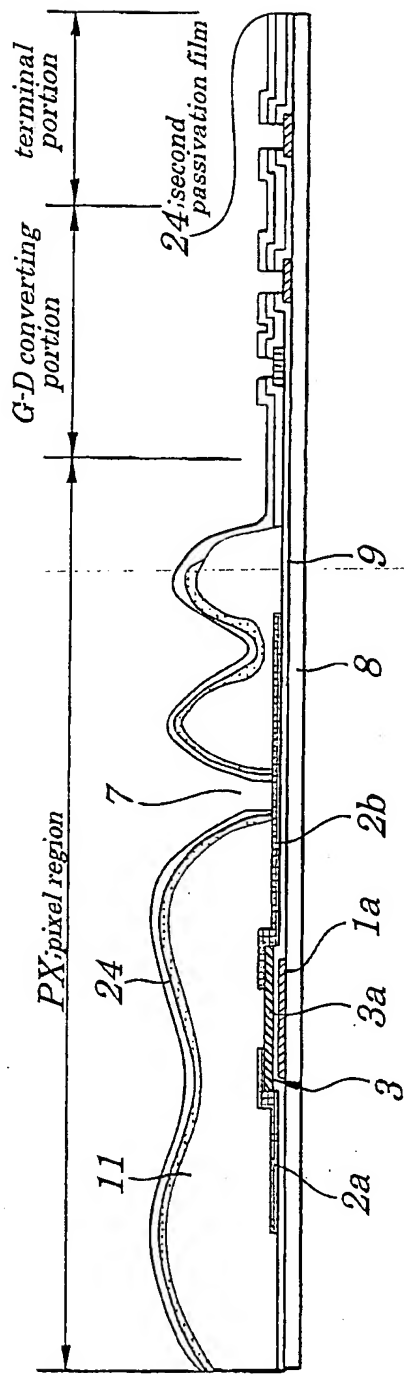


FIG. 21B

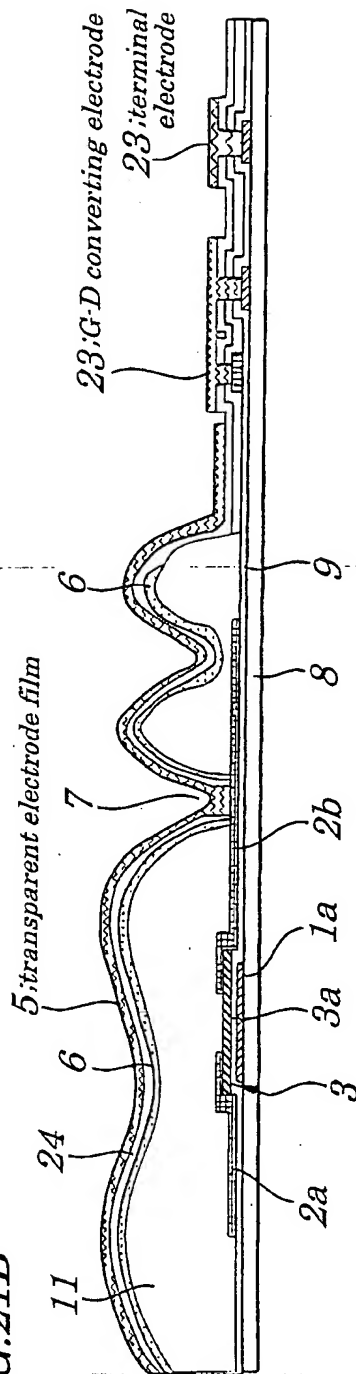


FIG. 22

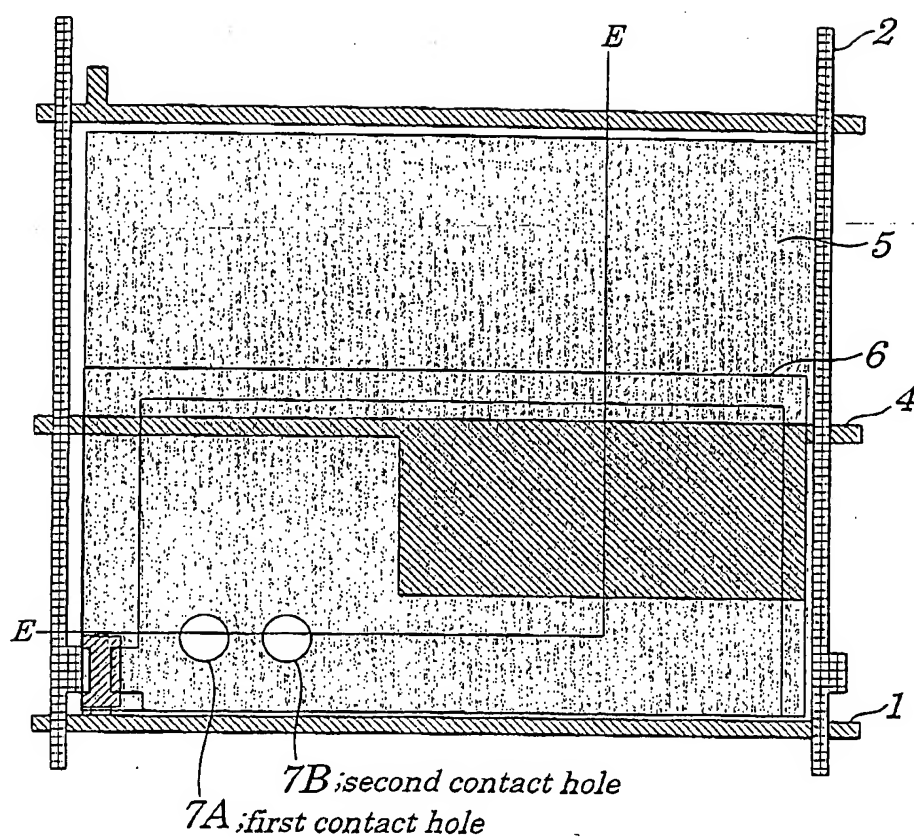
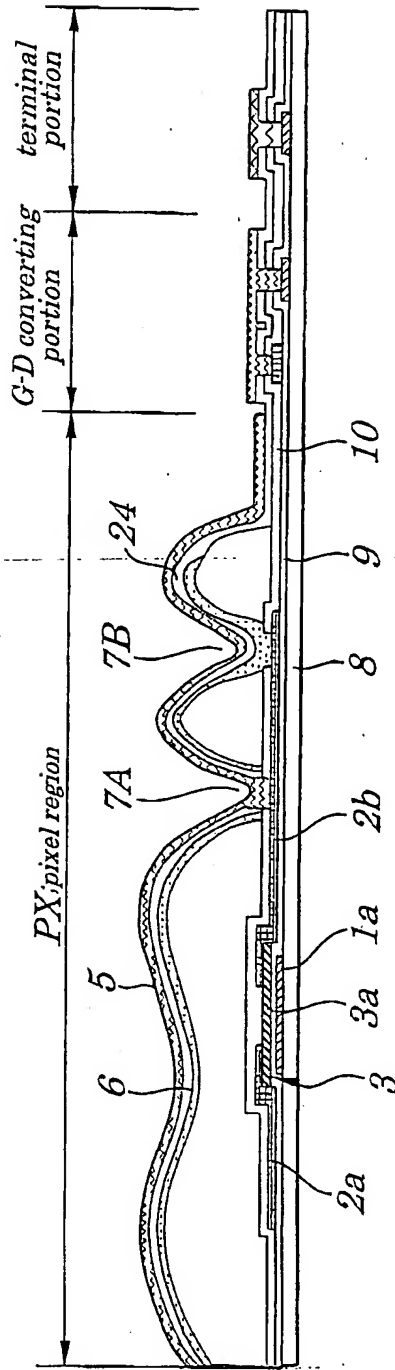
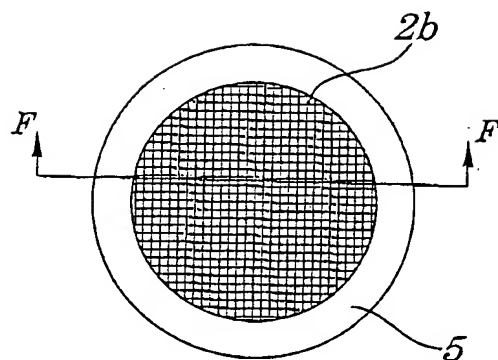


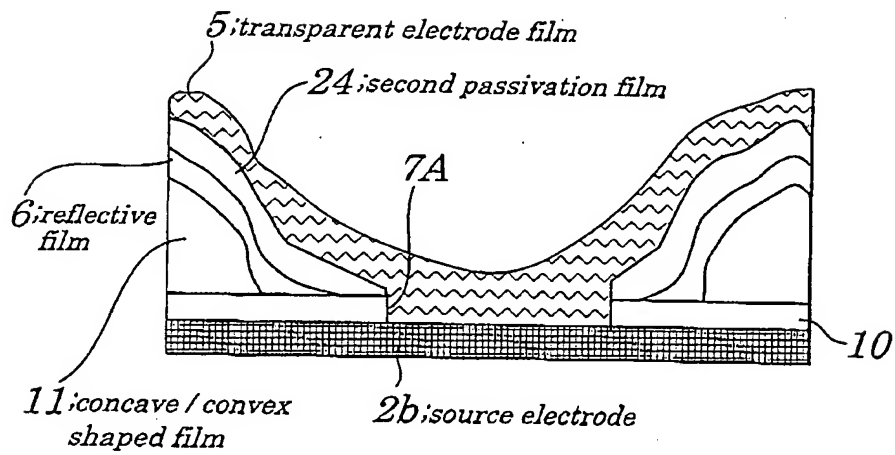
FIG. 23



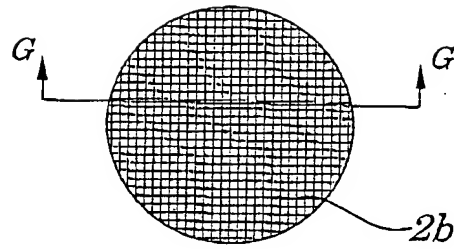
**FIG.24**



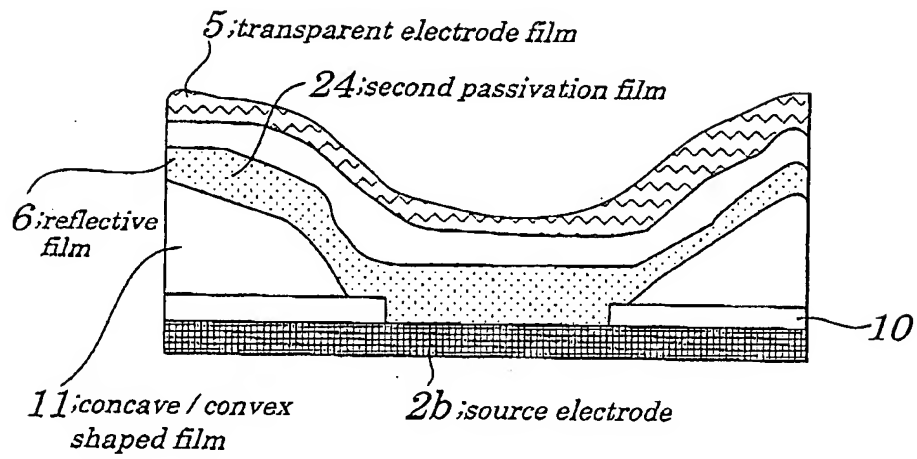
**FIG.25**



*FIG.26*



*FIG.27*



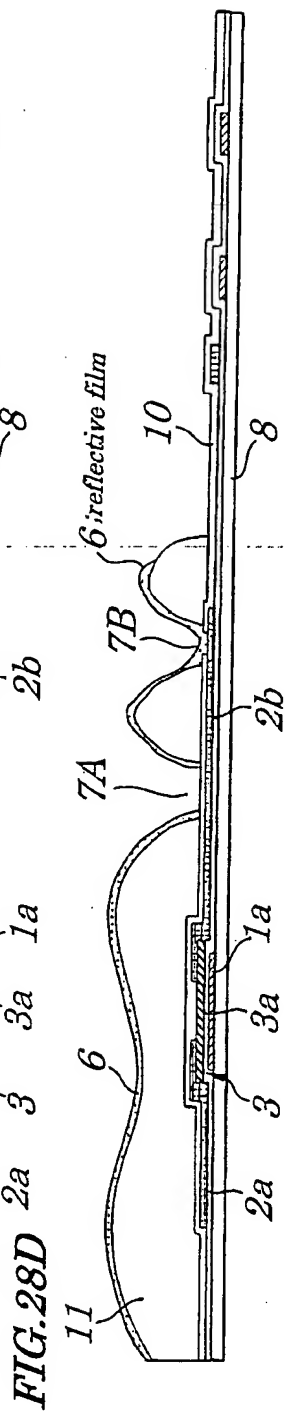
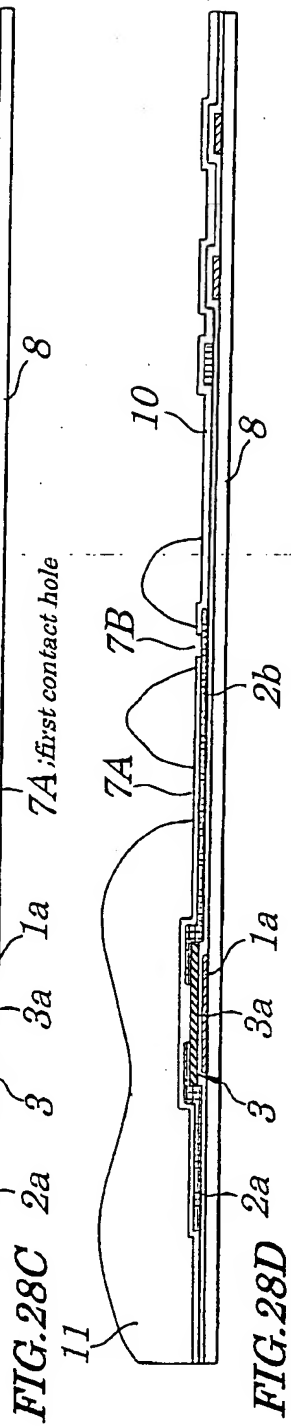
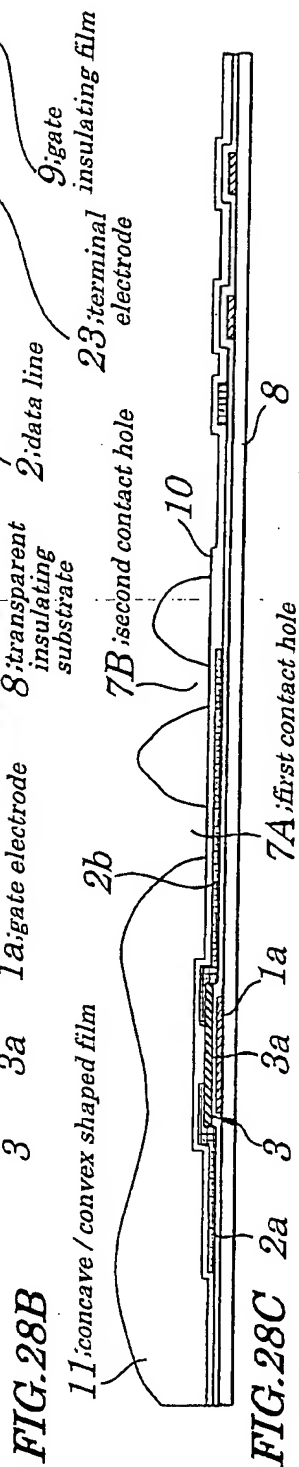
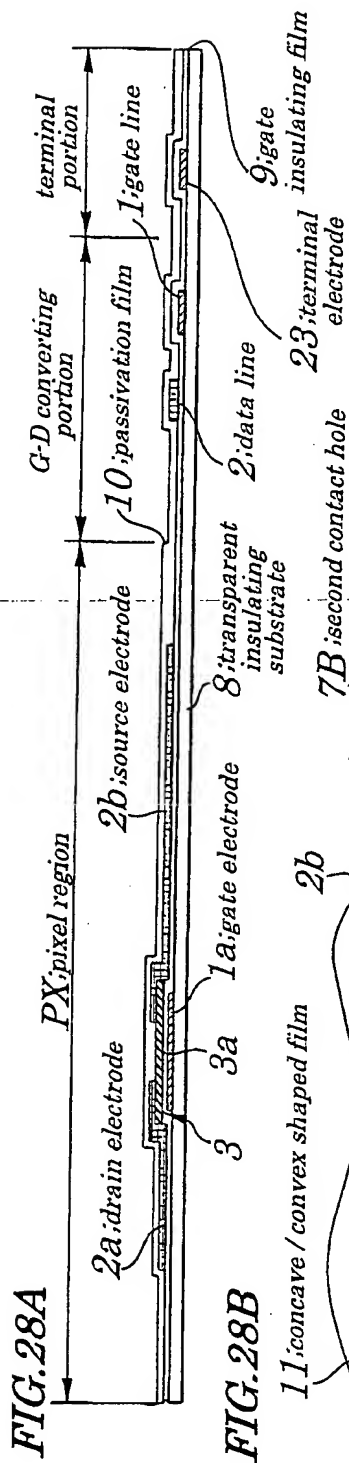




FIG. 29A

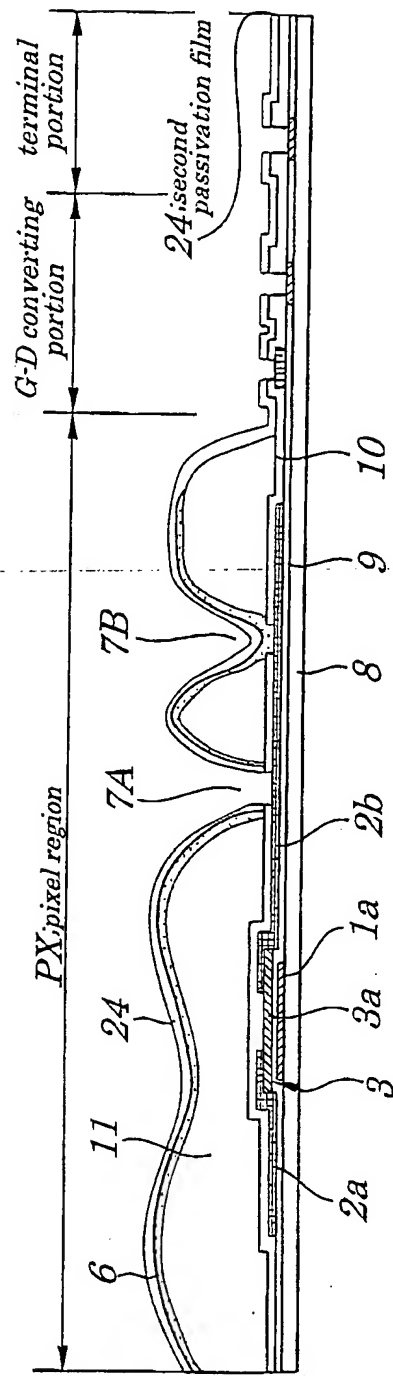


FIG. 29B

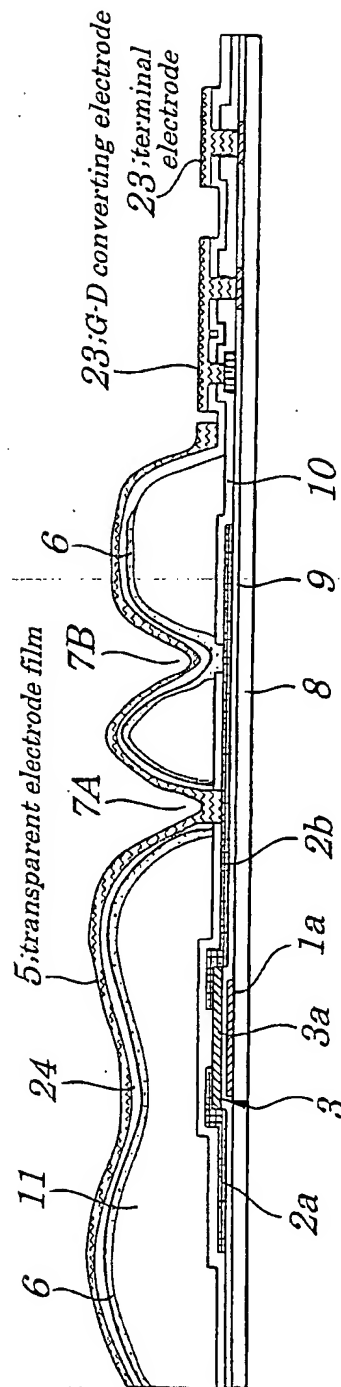
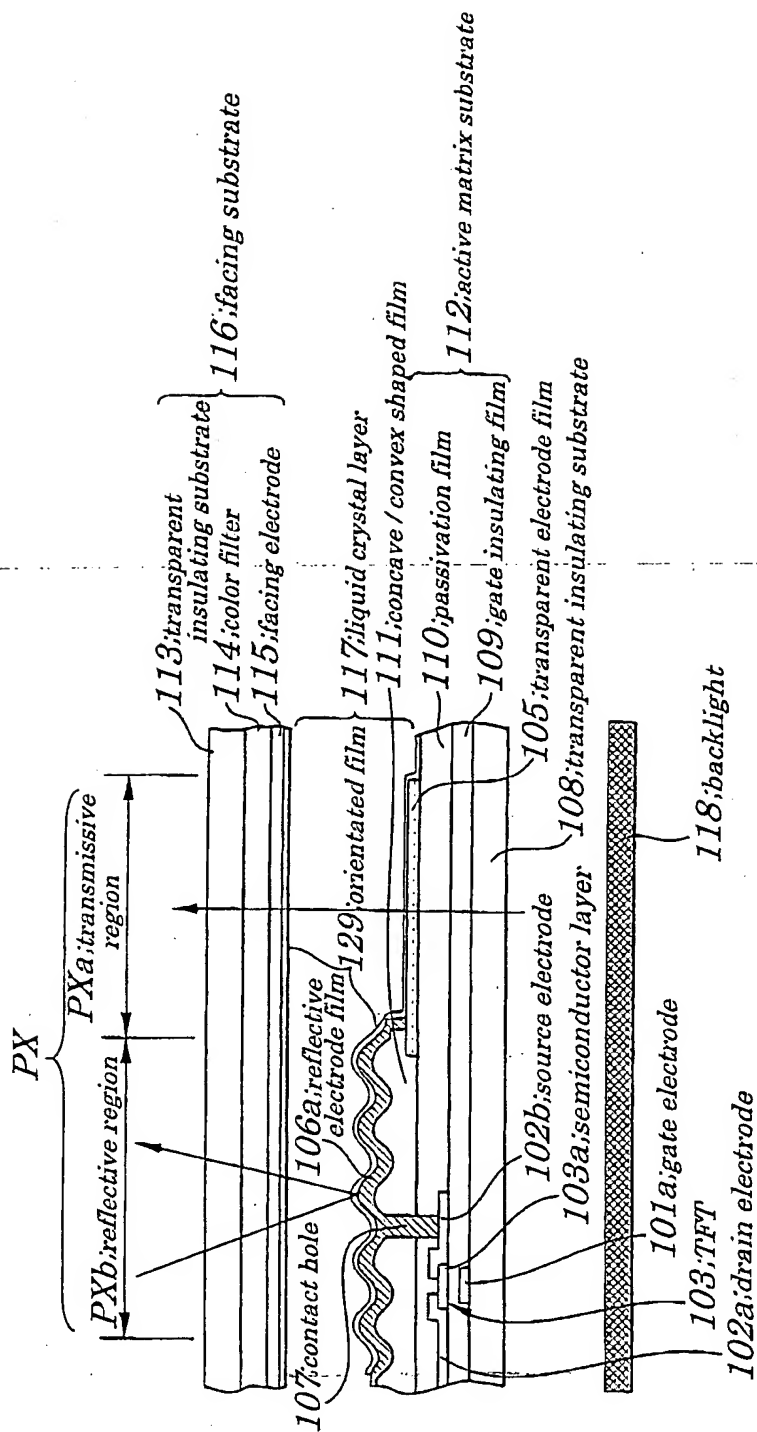
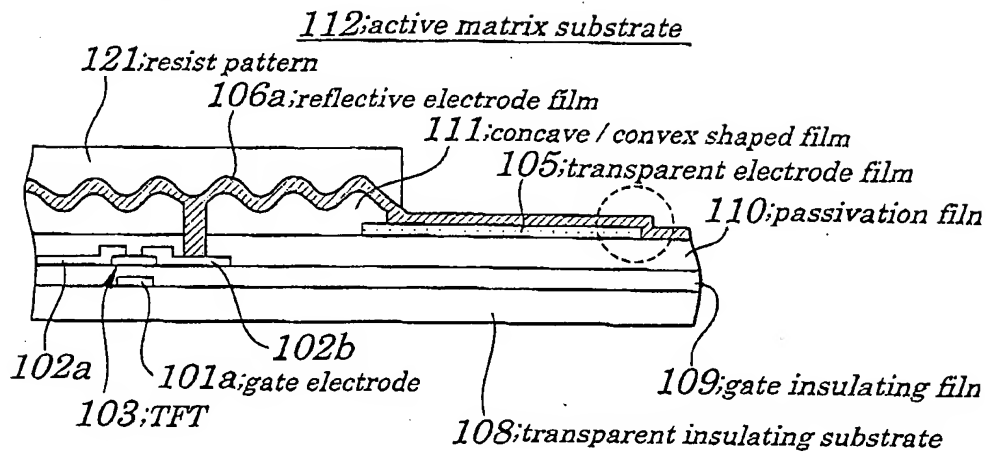


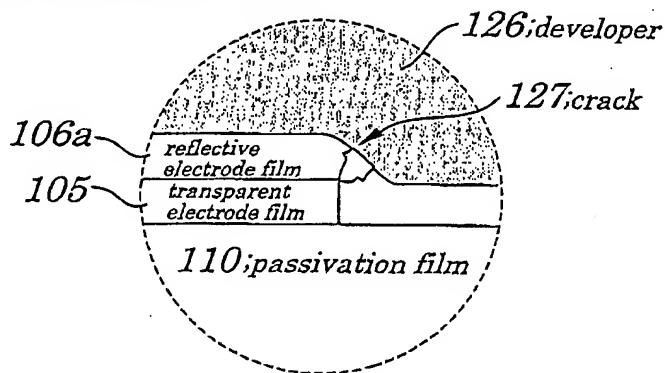
FIG. 30 (PRIOR ART)



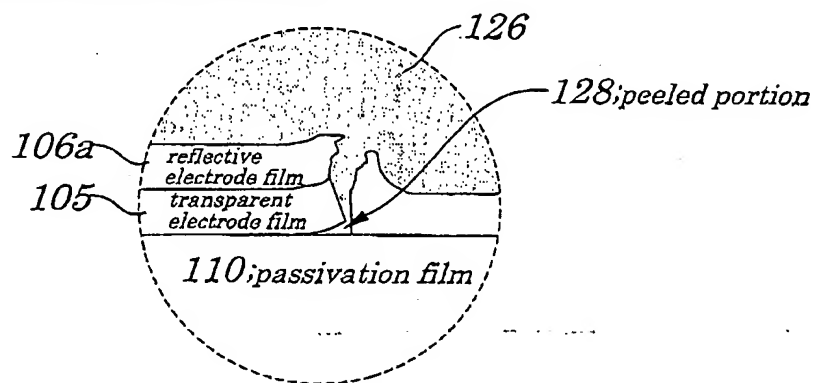
**FIG.31A(PRIOR ART)**



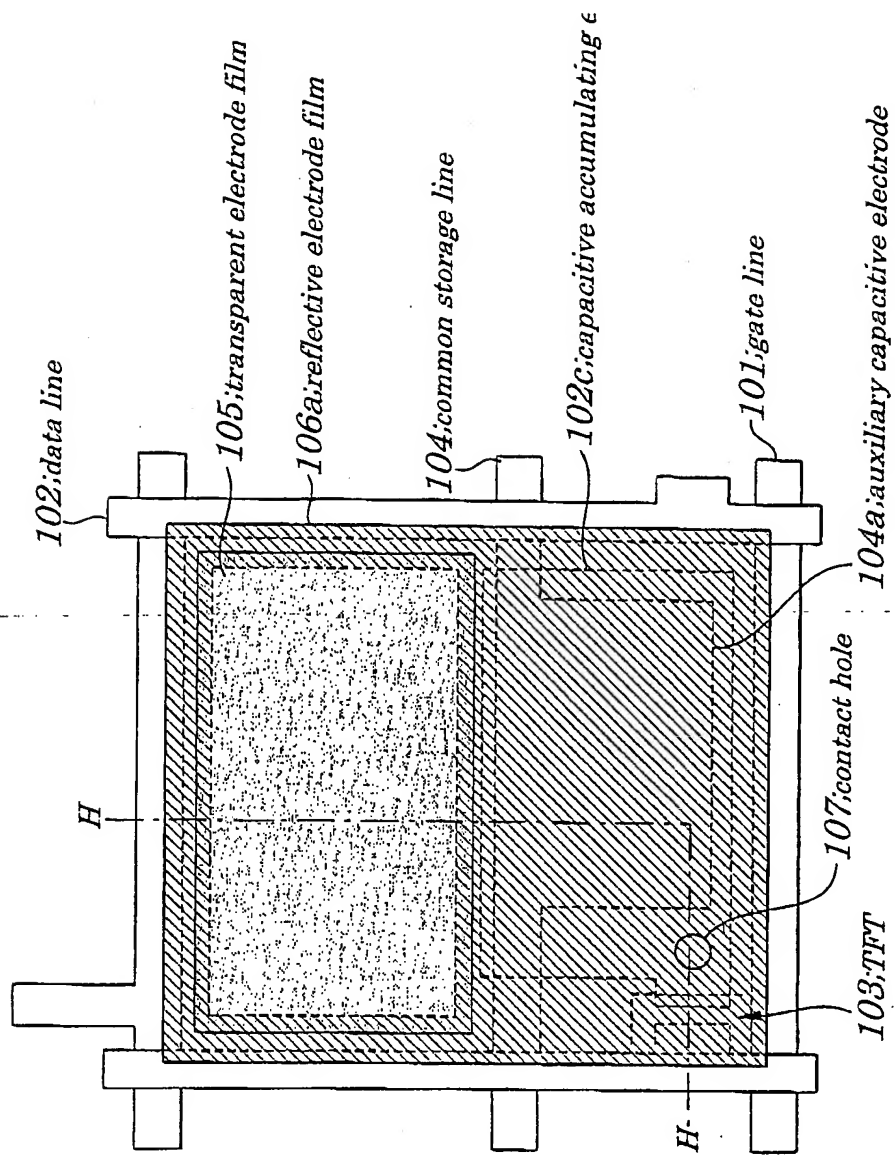
**FIG.31B(PRIOR ART)**



**FIG.31C(PRIOR ART)**



**FIG.32**



**FIG. 33**

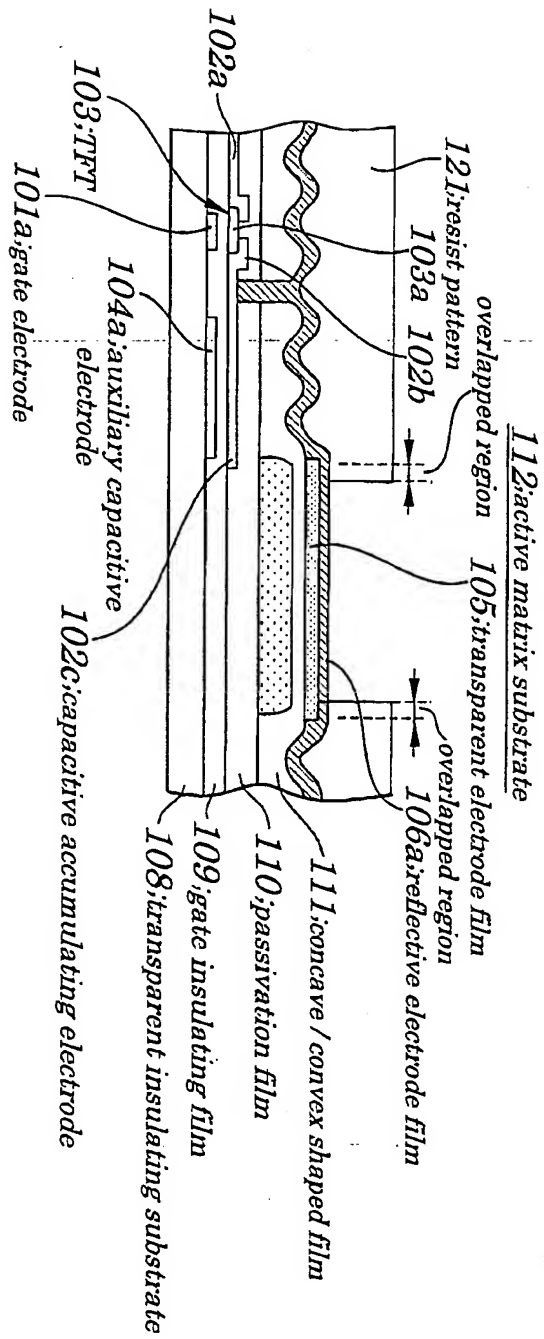
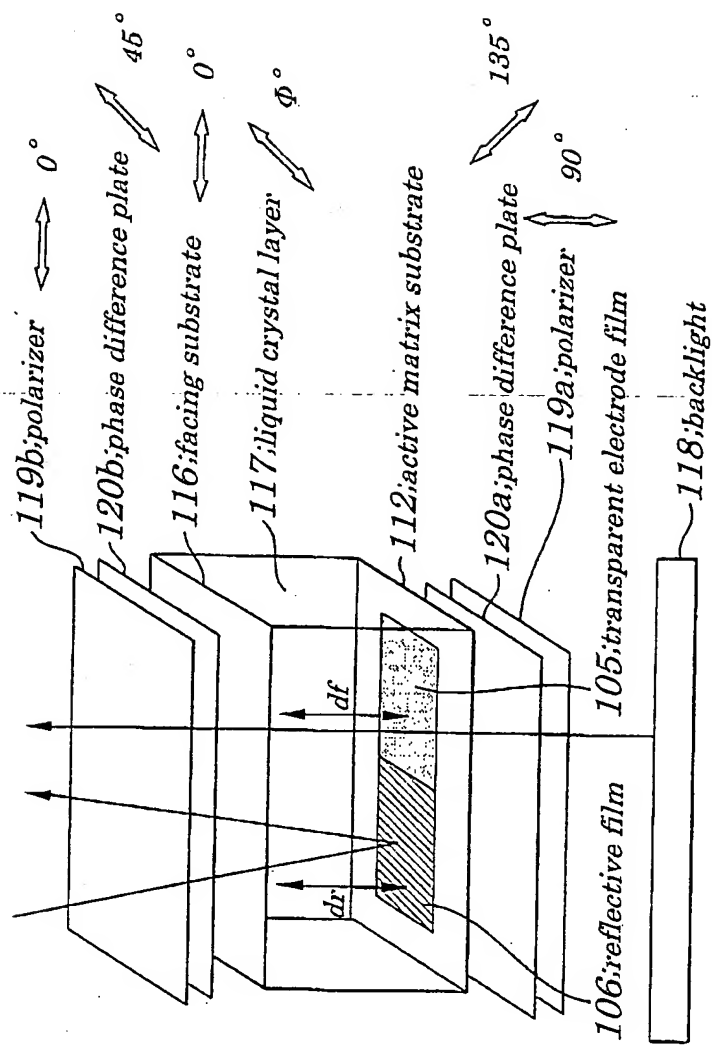
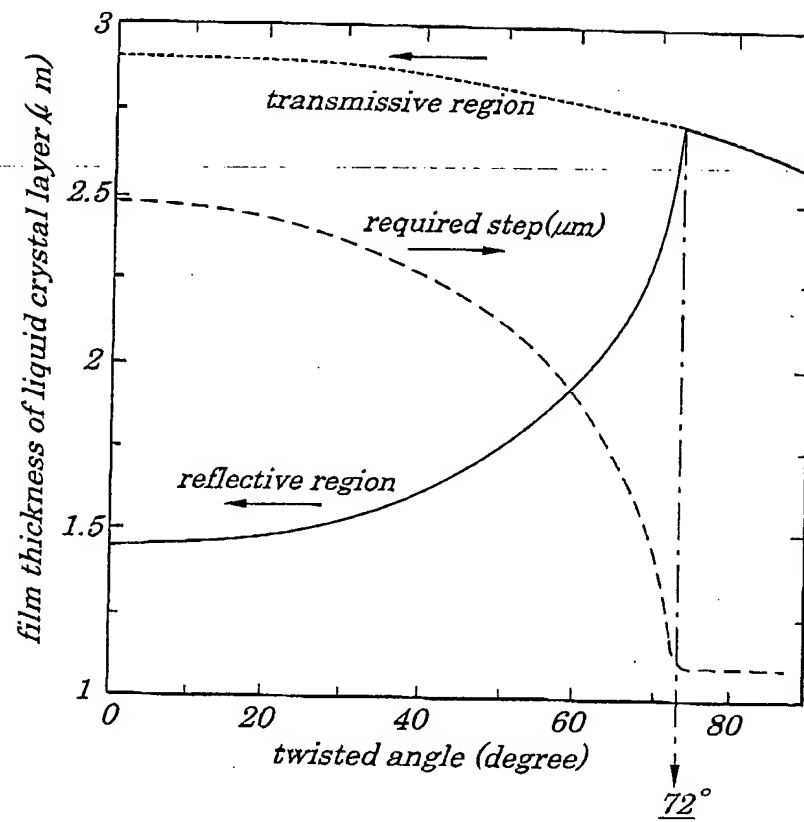


FIG. 34 (PRIOR ART)



**FIG.35 (PRIOR ART)**



**FIG.36 (PRIOR ART)**

